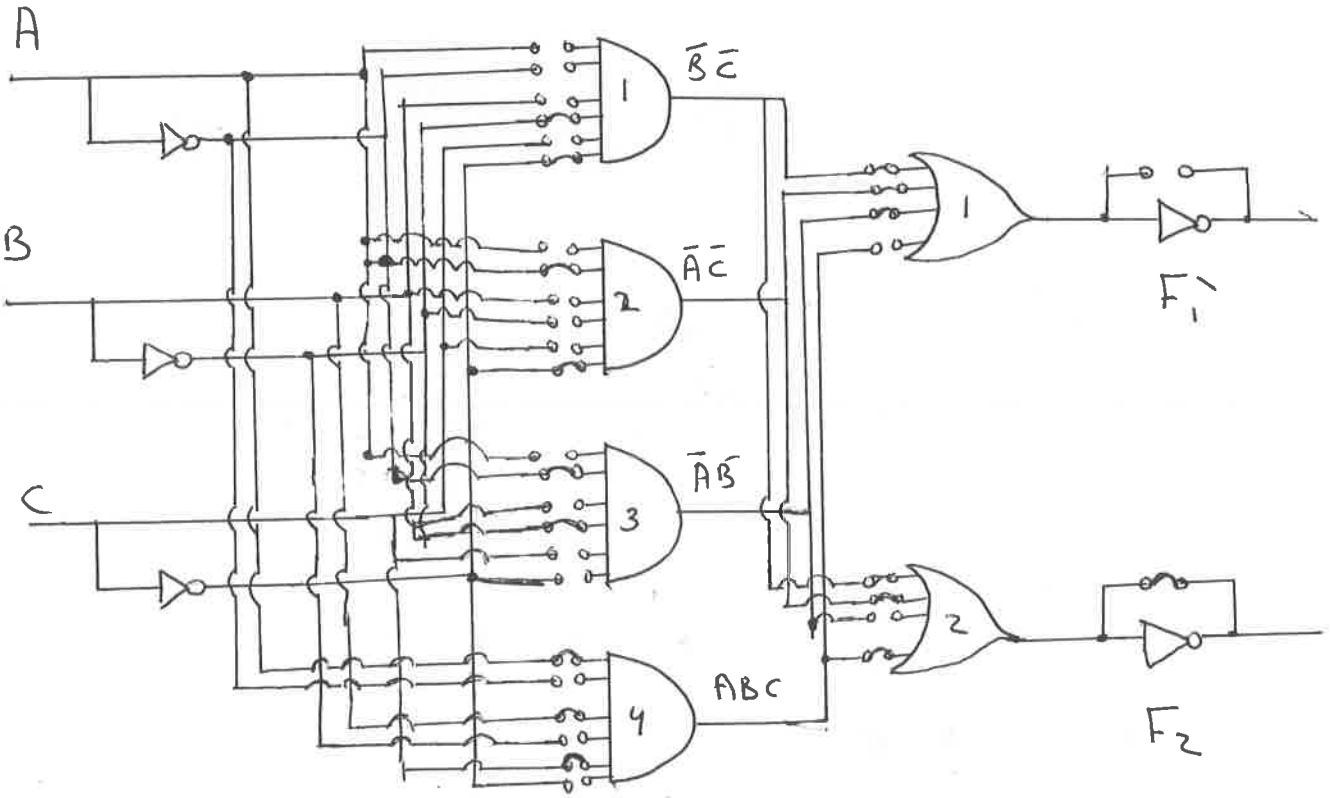
$$\therefore \quad F_1 = \underline{\bar{B}\bar{C}} + \underline{\underline{\bar{A}\bar{C}}} + \bar{A}\bar{B}$$

$$F_2 = \underline{\bar{B}\bar{C}} + \underline{\underline{\bar{A}\bar{C}}} + ABC$$



((PLA Logic ckt))

Synchronous Sequential Logic Circuits :-

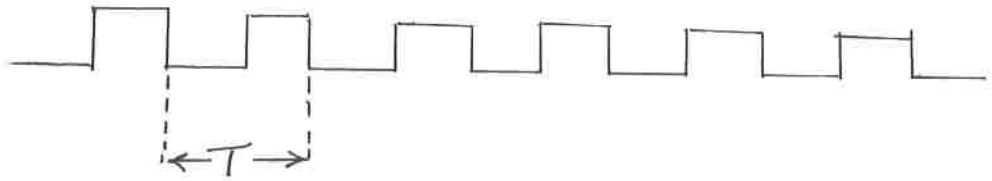
Up to now everything has been combinational, that is the o/p at any instant of time depends only on what the i/p's are at that time. (This ignores the small delay between the time the input of circuit changes and when the o/p changes).

A sequential systems :- It is a system that have memory, Thus, that output will depend not only on the present i/p but also on the past history what has happened earlier.

We will deal almost with clocked systems (sometimes referred to as synchronous).

A clock is just a signal that alternates (over time) between 0 and 1 at a regular rate. In the figure below, the clock signal is 0 half of the time and 1 half of the time.

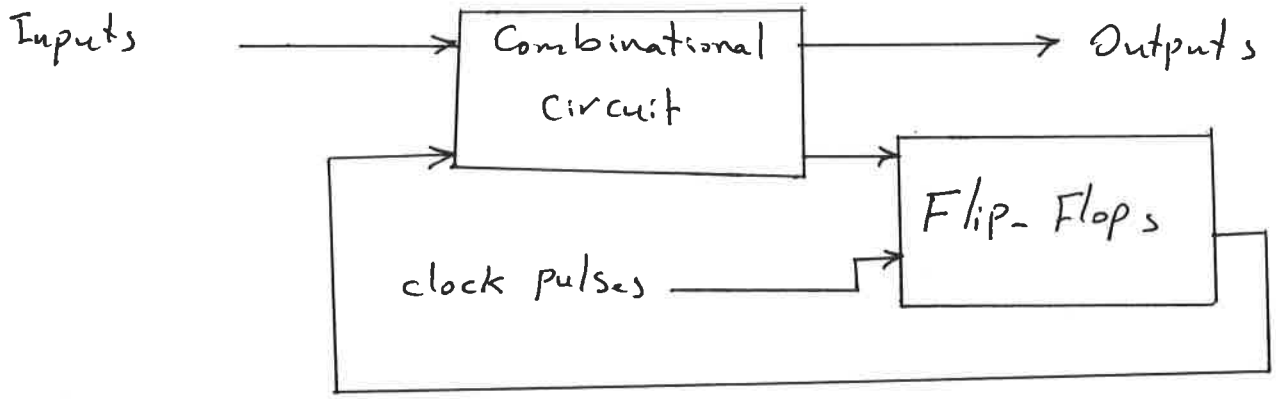
The period of the signal (T on the diagram) is the length of one cycle. The frequency is the inverse (1/T).



clocked Sequential circuits are the type most frequently encountered in practice.

The storage elements used in clocked sequential ccts are called Flip - Flops.

A Flip-Flops is a binary storage device capable of storing one bit of information. Sequential circuits may use many F.F's to store as many bits as necessary. The block Diagram of a synchronous clocked sequential system is shown below.



Latches :- It is the most basic types of Flip-Flops operate with signal levels. The latches are the basic circuits from which all Flip-flops are constructed. Although Latches are useful for storing binary information and for the design of asynchronous sequential Circuits.

A flip-flop is a clocked binary storage device, that is, a device that stores either a 0 or 1. Under normal operation, the value will only change on the appropriate transition of the clock. The state of the System (what is in memory) changes on the transition of the clock. For some flip-flops, that change

take place when the clock goes from 1 to 0; that is referred to as trailing-edge triggered. For others that changes takes place when the clock goes from 0 to 1; that is referred to as leading edge. triggered. Figures below show that.

- In general a combinational system,
  1- No feed back to the system from the output.
  2- No memory required.
- In general Sequential system,
  1- There is feedback to the input from output.
  2- It has a memory.

Flip-Flops :-

It is a cct that maintain a binary state until directed by an I/P signal, to switch state. The major difference between different types of flip-flop are:-

1- No. of I/P's they have.
2- The manner in which the i/p's effects the Binary state.

The F.F find wide application in Digital system such as:-

1- Counters.

2- Registores.

3- Memory.

4- control Logic.

Tyes of Flip-Flops:-

1- (S-R) Set-Reset Flip-Flop.

2- (J-K) Flip-Flop.

3. T (Toggle) Flip-Flop.

4- D (Delay) Flip-Flop.

1) (SR - F/F) (Set-Reset F.F) :-

The F.F has 2 staible state. It is capable of being on either a "high" state (Logic 1) or a "Low" state (Logic 0).

2 states are Set & Reset

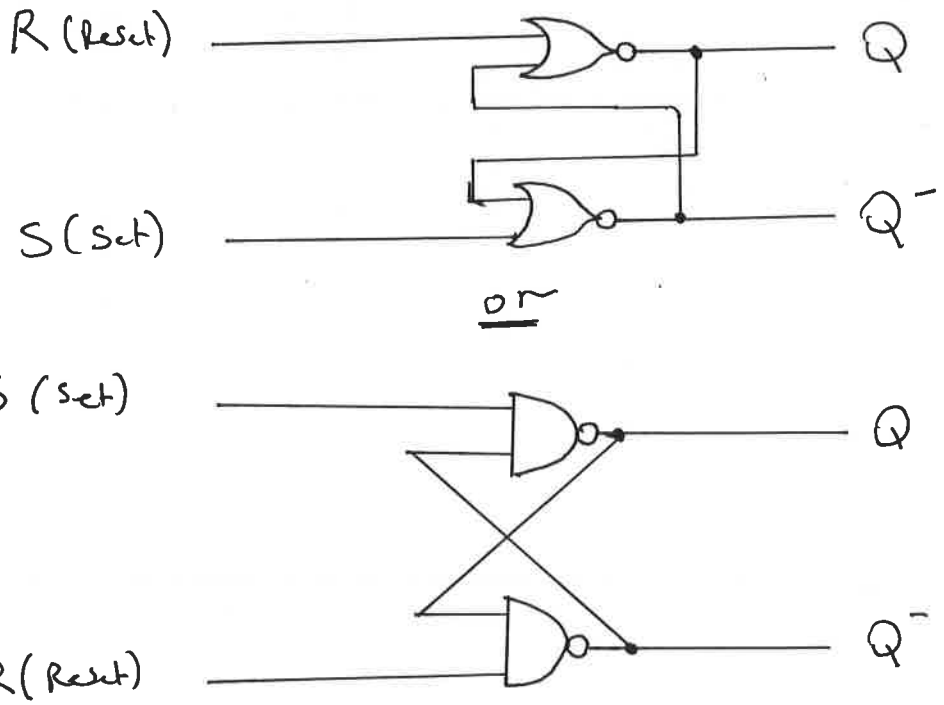
Set : Q output is Logic 1 set

$\bar{Q}$ output is Logic 0

Reset : Q output is Logic 0 Reset

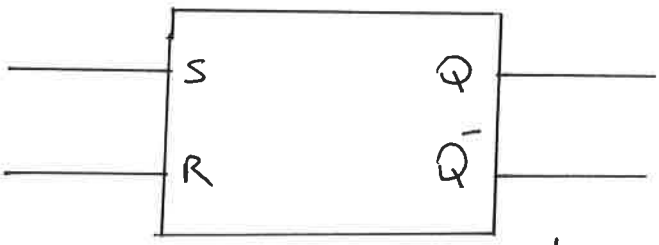
$\bar{Q}$ output is Logic 1

and S-R (Set-Reset) is formed with 2-cross-coupled NAND gates or 2-NOR gates



The o/p of NOR gate is (0) if any I/p is (1) and the o/p is (1) only when all inputs are (0).

The block Diagram of SR/F.F is :-



Block Diagram of (S-R)/F.F

The truth table of SR/F.F is :-

S	R	Q	
0	0	Last case	(No. change)
0	1	0	Reset
1	0	1	Set
1	1	X	Forbidden (Not allowed)

Bubbled and Gate :-

We can change the NOR gate to bubbled gate according to De-morgan's Theorm.

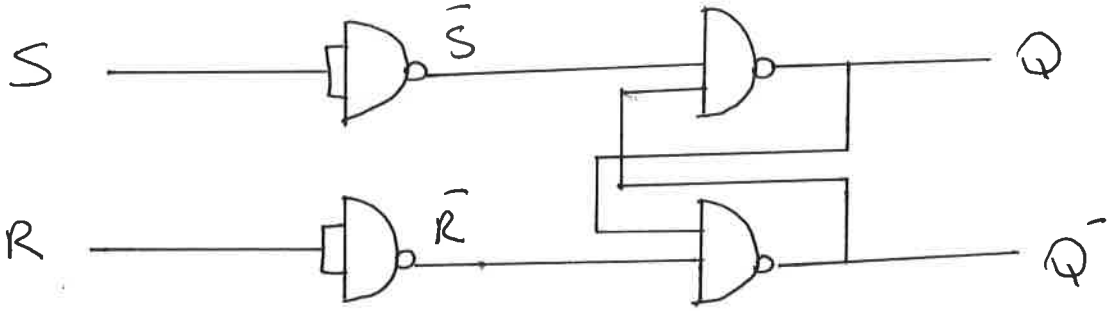
① 

$\overline{A+B} = \bar{A}\cdot\bar{B}$

② Bubbled OR :- We can change the NAND gate by bubbled gate such as:-

$\overline{AB} = \bar{A}+\bar{B}$; 

We can get SR/F.F from the (NAND) gates as shown below:-



S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

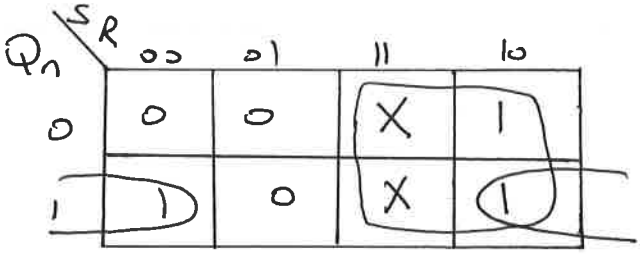
* Q_n i/p
* Q_{n+1} next output

We can Simplified the truth table to:-

S	R	Qn+1
0	0	Qn
0	1	0
1	0	1
1	1	X

The ch/s eq. of RS Flip-Flop is:-

$$Q_{n+1} = S + \bar{R} Q_n$$



There is another useful table called "Exition table"

S	R	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

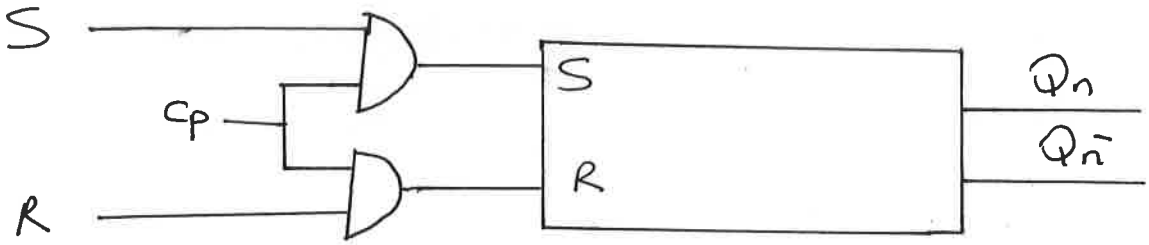
Qn	Qn+1	S	R
0	0	0	d
0	1	d	0
1	0	(0)	1
1	1	1	(0)

* d dont care

* (0) means SR are both are (1) not allowed, or both (1) in SR do not allowed.

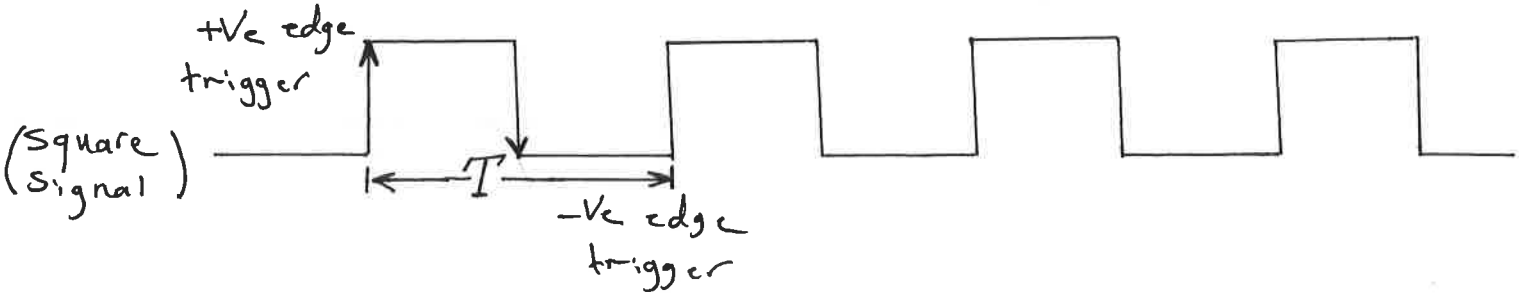
The clock SR/F.F

We can use the pluses (Synchronous pluses) in Digital systems to operat this system with clock, we can shown the clock pulse :-

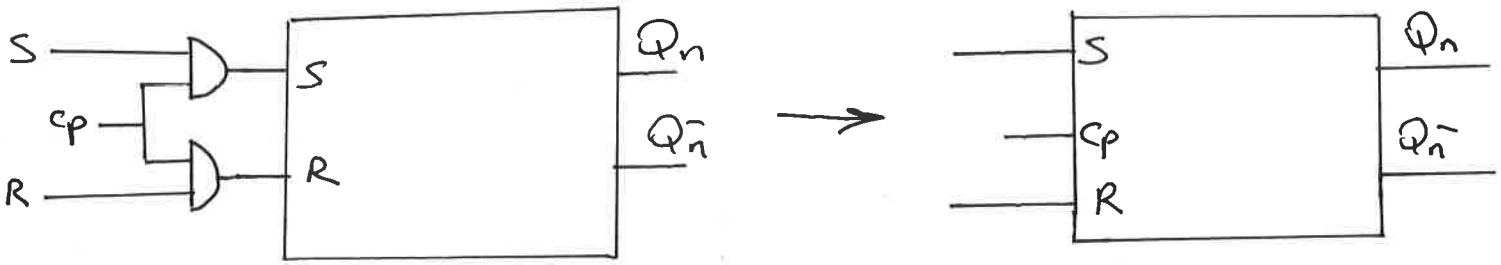


When:- (Cp=0) no change

(Cp=1) Apply (SR)



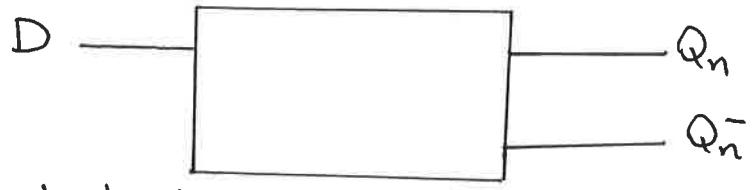
The clock SR/F.F

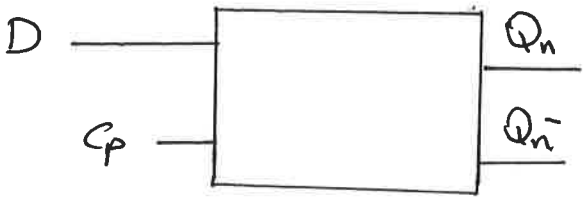


Cp	S	R	Q_{n+1}
0	0	0	} No change
0	0	1	
0	1	0	
0	1	1	
1	0	0	no change
1	0	1	0
1	1	0	1
1	1	1	X

D Flip- Flop :-

It is the most economical and efficient Flip-Flop constructed. Because it required the smallest number of gates. The name comes from Delay, Since the o/p is just the i/p delayed until the next active clock transition. Block Diagram of D/f.F is shown below :-

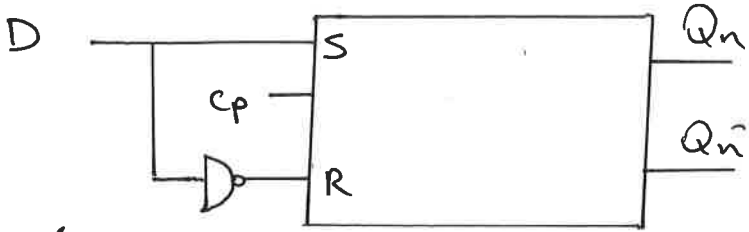




The truth table:-

D	Q_{n+1}
0	0
1	1

We can use the SR/F.F to build the D/F.F., Use the (NAND) gate as Not to prevent ((1, 1)).



When:- (D = 0), S = 0, R = 1, $Q_{n+1} = 0$

(D = 1), S = 1, R = 0, $Q_{n+1} = 1$

* As the (S) and (R), one reverse the other, So the (D = 1), make the F.F in (Setting),
* If the (D = 0), make the F.F in (Resitting), & the S, R can not be 1 for any case.